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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,178	02/12/2004	Andreas Jakobs	0928.0025C	3088

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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,178	JAKOBS, ANDREAS	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *2-4 and 12-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-11,15 and 17-20* is/are rejected.

7)☒ Claim(s) *6 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-12-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on February 12, 2004 was filed in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner. The references referred to in the IDS submitted June 01, 2004 have been considered but are listed in the attached Notice of Reference Cited (PTO-892) since no form PTO-1449A accompanied those references.

Election/Restrictions

3. Claims 2 – 4 and 12 – 14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions, there being no allowable generic or linking claim. Applicant's election without traverse of claims 5, 6, 15, and 16 (group III) in the reply filed on November 03, 2005 is acknowledged.

4. Claims 1, 5 – 11, and 15 – 20 are pending.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 5, 7, 8, 10, 11, 15, 17, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al. (US Pat 5,731,945) in view of Longwell et al. (US Pat 6,385,113 B1).

Regarding **claims 1 and 11**, Bertin et al. disclose a memory module (figs. 13 or 14), comprising:

a mounting substrate (boards 200 or 205);

a plurality of integrated memory components (201 or 206) arranged on the mounting substrate;

a refresh control circuit which is arranged separately from the memory components on the mounting substrate, an output of the refresh control circuit being connected to the plurality of integrated memory components (col. 5, lines 12 – 41, peripheral circuitry, or I/O circuitry, which includes circuits for the RAS/CAS, read/write controls, and also refresh controls, is moved to form a separate logic chip. Hence, the refresh control circuit is arranged separately from the memory components.);

the mounting substrate having connections for supplying address and command signals (204 or 210).

Although Bertin et al. did not clearly show the refresh control circuit having input for receiving external commands, and independently generating refresh command and transmit the refresh command for refreshing the memory components, the feature has been taught by Longwell et al. (fig. 6 shows a refresh controller 14, which receives inputs LOAD signal 68 and refresh request 16 externally, and generates refresh outputs 40, including Adddress, RAS, and CAS signals, to the memory components. Since the outputs 40 also depends on counter 80 and time controller 84, which are internal to the refresh controller 14, the output commands from 40 are independent from the inputs 15 and 68).

Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the refresh controller taught by Longwell et al. to Bertin et al.'s memory modules, which feature separate peripheral circuit including refresh control circuit, so that at an appropriate time, the time controller 84 will generate an IRAS and ICAS signals to be used as normal RAS, depending on the memory components' characteristics (col. 9, lines 10 – 53).

Regarding **claims 5 and 15**, Bertin et al. and Longwell et al. disclose the memory module as claimed in claim 1 or 11, wherein

the memory components each having a memory cell array organized in a form of a matrix, the array having rows and columns (inherent in memory art), and

the refresh control circuit ascertaining which rows in a selected memory component have not been accessed in a predefined period of time and, based on this evaluation, independently determine when to send a refresh command (figs. 7 – 10,

abstract: "..., a refresh controller accesses a look up table to store data indicated the status of memory cells. Prescaling may then adjust the period and duty cycle of the refresh cycle in ...". See also col. 10, line 40 – col. 11, line 65. Accordingly, the refresh commands are independently controlled, depending on the status of the memory cells, with their corresponding rows/columns whose addresses are accessed by the refresh controller).

Regarding **claims 7 and 17**, Bertin et al. and Longwell et al. also disclose the memory module as claimed in claims 1 and 11, wherein the refresh control circuit is arranged within a semiconductor chip, which is separate from the memory components (Bertin et al.: col. 7, lines 1 – 3).

Regarding **claims 8 and 18**, Bertin et al. and Long well et al. also disclose the memory module as claim in claims 1 and 11, wherein the input connection of the refresh control circuit is connected to a contact strip on the memory module (since the refresh controller is now arranged on a separate chip in the module as shown above, it is therefore considered inherent that the input connection of the refresh controller is connected to a contact strip on the memory module!).

Regarding **claims 10 and 20**, Bertin et al. also disclose the memory module as claimed in claims 1 and 11, wherein the memory components in the memory module are dynamic read/write memories (col. 3, lines 38 – 42).

7. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al. and Longwell et al., and further in view of Doblar et al. (US Pat Pub 2003/0090879 A1).

Regarding **claims 9 and 19**, Bertin et al. and Longwell et al. disclose the memory module as claimed in claims 1 and 11, except wherein the memory module is in the form of a DIMM arrangement. Nonetheless, this feature has been taught by Doblar et al. (paragraph 0004). Therefore it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature taught by Doblar et al. to the disclosures by Bertin et al. and Longwell et al. so that higher signal density may be accommodated due to two contact pads of DIMMs.

Allowable Subject Matter

8. **Claims 6 and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

The prior arts fail to teach or reasonably suggest the memory module, further including a respective set of counter circuits for independently operating units of rows, the individual counter circuits in a set being associated with a respective different row in the corresponding unit of rows, the respective counter circuit being reset when the

associated row is accessed, the refresh control circuit evaluating the counter circuits with respect to the count and based on this evaluation, independently determining when a refresh command will be sent.

10. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See US Pats 5,345,574 and 5,959,923 for refresh controllers of particularly relevance, and US Pat Pub 2004/0027876 for feature providing refresh control circuit mounted on a separate chip from the memory chips.

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D Pham
November 11, 2005

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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